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Comparison between Radix-2 and Radix -4 based on Booth Algorithm

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Abstract: This paper presents the implementation and comparison of high speed multipliers which depends on booth encoding. In this, we compare the performance of Radix-2 and Radix-4 based on booth multipliers. The multipliers are designed for 8X8 bit multiplication operation. We proposed designs of Booth algorithm which is called Modified Booth algorithm using Radix -4 has been designed using VHDL and synthesized, implemented using Xilinx ISE Sparten 3 Board. We compare the terms according to the critical path delay, cost, area and power consumption.

Keywords: Basic Booth Multiplier using Radix-2, Modified Booth Encoding using Radix-4.

I. INTRODUCTION

In many real-time DSP applications, high performance is critical condition. Multipliers are key components of many high performance systems where the complex arithmetic operations are happened such as Digital Signal Processor, Calculator, Microprocessor and FIR Filters. Multipliers are very important circuits in systems because overall performance of system depends on it. But multipliers usually have large area, longer delays and consume more power. Hence optimizing the speed, area and power of the multiplier is major design issue in Digital Signal processing (DSP).The common multiplication method is "add and shift". In parallel multipliers number of partial products to be added is the main parameter that determines the performance of the multiplier Multiplication operation involves two major steps:

1) Generation of partial products
2) Adding of partial products.

The speed of multiplication can be improved by two ways.

1) Reducing the number of partial products.
2) Accelerating the summation of partial products.

II. BOOTH ALGORITHM

Booth algorithm was first implemented by Andrew Donald Booth 1950. In normal Booth's algorithm is an efficient hardware implementation of a digital circuit that multiplies two binary numbers in two's complement notation. Booth multiplication is a fastest technique that allows for smaller, faster multiplication circuits, by recoding the numbers that are multiplied.

The Booths multipliers widely used in ASIC oriented products due to the higher computing speed and smaller area. In the binary number system the digits, called bits, are to the set of {0,1}.The result of multiplying any binary number by binary bit is either 0 or original number. This makes the formation of partial products are more efficient and simple. Then adding all these partial products is time consuming task for any binary multipliers. The entire process consists of three steps partial product generation, partial product reduction and addition of partial products in Fig.(1) shown.

But in Booth multiplication, partial product generation depends upon the recoding scheme e.g.Radix-2 encoding. Multiplication using normal Booths recoding algorithm technique based on the partial product can be generated for group of consecutive 0's and 1's which is called Booths recoding. This recoding algorithm is used to generate efficient partial product. This increase in the width of partial product usually depends upon the radix scheme used for recoding. So, these scheme uses less partial product generation which in turn provides low power and area than Normal Booth Multiplier.

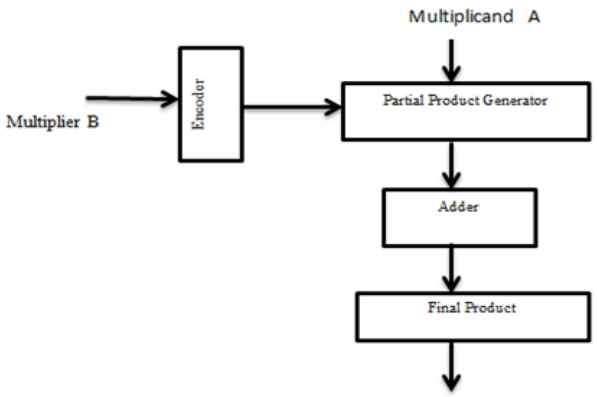

Fig.Block diagram of booth multiplier

RADIX-2 PROCEDURE:

1) Add 0 to the LSB of the multiplier and make the pairing of 2 from the right to the left which shown in the Fig.(2)
2) With 00 and 11 do nothing according to the encoding table.
3)01: mark shows the end of the string' of 1 (according to the table) and add multiplicand to the partial product.

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Table I Booth Encoding Table

yi	Yi-1	Zi-i	Multiplier Value	Situation
0	0	0	0	String of 0s
0	1	1	+1	End of string of 1s
1	0	1	-1	Beginning of string of 1s
1	1	0	0	String of 1s

4)10: mark shows beginnings of the string of 1 subtract multiplicand from partial product.st be indented. All

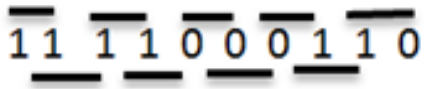

Fig.2. 2- Bit pairing as per Booth recoding using Radix- 2.

Modified Booth Multiplier using Radix -4:
The disadvantages of Booth Multiplier with Radix-2 is overcome by using the Modified Booth Multiplier with Radix-4 which reduces the half of the partial products in multipliers.

In Radix-4, encoding the multiplicands based on multipliers bits. It will compare 3-bits at a time with overlapping technique. Then the grouping starts from the LSB and the first block contains only two bits of the multipliers and it assumes zero for the third bit. These group of binary digits are according to the Modified Booth Encoding Table and it is one of the numbers from the set of (-2,2,0,1,-1).

Modified Booth multiplication is a technique that allows for smaller, faster circuits by recoding the numbers that are multiplied. It is standard technique used in chip design, and provide significant improvement over long multiplication technique.

Radix-4 Procedure:
1)Add 0 to the right of the LSB of the multiplier.
2)Extend the sign bit 1 position if it is necessary when n is even.
3)The value of each vector ,the partial products are coming from the set of (-2,2,0,1,-1).

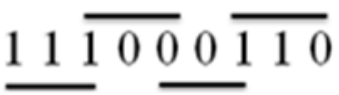

Fig. Grouping of 3-bit as per booth recoding

Table .II Modified Booth Encoding Table

Binary Numbers				MB Encoding			Input
Y_{2j+1}	Y_{2j}	Y_{2j-1}	y_j^{MB}	Sign(Sj)	Onej	Twoj	Carry
0	0	0	0	0	0	0	0
0	0	1	+1	0	1	0	0
0	1	0	+1	0	1	0	0
0	1	1	+2	0	0	1	0
1	0	0	-2	1	0	1	1
1	0	1	-1	1	1	0	1
1	1	0	-1	1	1	0	1
1	1	1	0	1	0	0	0

III. EXPERIMENTAL WORK

After analysing both multipliers .and compare their characteristics in terms of multiplication speed ,no of computations required ,no of hardware ,we come on finding that radix 4 booth multipliers is better than Radix 2 booth multipliers. By implementing both Radix 2 and Radix 4 multiplier we analysis that Radix multiplier computation speed is higher than Radix 2.We have done the coding of both multipliers separately in VHDL and simulate it to get the accurate waveforms as output of each multiplier .The simulation design result of Radix 4 is same as Radix 2 but only difference is that the synthesis report.

TABLE .III Analysis of Radix-2 and Radix-4

Device Utilization Summary	Radix-2	Radix-4
Number of slices	397	71
Number of 4 inputs LUTs	184	100
Number of bonded INPUT	16	16
Number of bonded OUTPUT	16	16
Macro statistics		
Latches	24	12
8 bit latch	24	12
XOR	71	23
1 bit xor2	64	21
8 bit xor2	7	2
Timing Summary		
Minimum Period	5.45ns	4.750ns
Minimum input arrival time before clock	7.93ns	4.01ns
Minimum output required time after clock	6.216ns	6.205ns

IV. CONCLUSION

In this paper we compare the performance of Booth multiplier with Radix 2 and 4. The implementation of the algorithm with an architecture and logic design is presented where in the delay, cost, power and hardware complexities of the design are compared to the recent designs. The delay and gates of Radix 4 are reduced and

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the processing speed is increased than the Radix 2. We calculated speed and area using Xilinx tool and obtained simulation.

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